REMARKS

This responds to the Office Action mailed on June 23, 2005, and the references cited therewith.

Claims 1, 2, 5 and 8 are amended, claims 9-27 are canceled, and claims 28 and 29 are added; as a result, claims 1-8, 28 and 29 are now pending in this application.

Affirmation of Election

Restriction to one of the following claims was required:

I. Claims 1-8, drawn to utilizing memory based TLB, classified in Class 711 subclass 207.

II. Claims 9-26, drawn to controlling transfer of block of data, classified in Class 710, subclass 23.

III. Claim 27, drawn to archiving data, classified in Class 714, subclass 2.

As provisionally elected by Applicant's representative, Thomas F. Brennan, on June 20, 2005, Applicant elects to prosecute the invention of Group I, claims 1-8.

The claims of the non-elected invention, claims 9-27, are hereby canceled. However, Applicant reserves the right to later file continuations or divisions having claims directed to the non-elected inventions.

Objections to the Specification

The specification has been amended to change the title and to add a missing serial number, as required.

§103 Rejection of the Claims

Claims 8, 1, 4, 5, and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaiser et al. (EP0766177A1) in view of Peck, Jr. et al. (US 6,686,920).

Kaiser describes an information-handling system in which address translation occurs in the memory controller. Peck describes a memory translation mechanism which can be used when multiple processors are accessing a single memory.

In contrast, Applicant describes a multiprocessor system in which the translation look-aside buffers are distributed across a plurality of memory sections. Claims 1 and 3-8 have been amended to clarify this distinction.

Claims 2, 3 and 6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kaiser et al. (EP0766177A1) in view of Peck, Jr. et al. (US 6,686,920), further in view of Herrell et al. (US 5,301,287).

Applicant describes a multiprocessor system in which a FIFO accepts memory commands from two or more of the processing elements and transmits each of the memory commands to at least one of the processor translation look-aside buffers. None of the cited references describe such a system. Claim 2 has been amended to clarify this distinction.

Finally, claims 3 and 6 are patentable since they are dependent on patentable base claims for the reasons given above.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

ROGER A. BETHARD

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6909

Date December 22, 2005

By Thomas J. Brennan
Thomas F. Brennan
Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of December, 2005.

CANDIS BUENDING
Name

Candis Buending
Signature